WHAT IS CLAIMED IS:

1. An on-screen display unit comprising:

a CPU for generating data to be subjected to OSD (on-screen display);

first and second OSD RAMs each for storing the data to be subjected to OSD in one of OSD blocks;

a memory bus for transferring the data to be stored in said first and second OSD RAMs in synchronization with an operation clock signal of said CPU;

an OSD local bus for transferring the data stored in said first and second OSD RAMs to be used for the OSD in synchronization with an OSD clock signal;

a register to which said CPU sets a switching bit;

a switch for connecting said first OSDRAM to said memory bus and said second OSDRAM to said OSD local bus in response to the setting of the switching bit; and

OSD control circuit for generating an interrupt signal to said CPU at an end of OSD of the data stored in said second OSDRAM, wherein

said CPU, receiving the interrupt signal, sets the switching bit of said register such that said switch connects said second OSDRAM to said memory bus and said first OSDRAM to said OSD local bus, and supplies said memory bus with subsequent data.

2. An on-screen display unit comprising:

an OSD (on-screen display) RAM for storing data to be subjected to OSD;

a memory bus for transferring data to be stored in said OSD RAM;

a buffer for storing data read from said OSD RAM;

an OSD local bus for transferring data in said buffer to be subjected to the OSD; and

a buffer transfer control circuit for reading data necessary for the OSD on a horizontal scanning line from among the data stored in said OSD RAM and storing the data to said buffer, and for writing data from said memory bus to said OSD RAM during transfer of the data stored in said buffer to said OSD local bus.

3. The on-screen display unit according to claim 2, wherein said buffer transfer control circuit reads the data necessary for the OSD on a current horizontal scanning line and stores the data in said buffer, during a section on the current horizontal scanning line before making the OSD on the current horizontal scanning line.

4. The on-screen display unit according to claim 2, wherein said buffer transfer control circuit reads the data necessary for the OSD on a next horizontal scanning line and stores the data in said buffer, during a section on the current horizontal scanning line after making the OSD on the current horizontal scanning line.

5. The on-screen display unit according to claim 2, wherein said buffer transfer control circuit selects one of a first operation mode and a second operation mode, wherein in the first operation mode said buffer transfer control circuit reads the data necessary for the OSD on a current horizontal scanning line and stores the data in said buffer during a section on the current

horizontal scanning line before making the OSD on the current horizontal scanning line, and wherein in the second operation mode said buffer transfer control circuit reads the data necessary for the OSD on a next horizontal scanning line and stores the data in said buffer during a section on the current horizontal scanning line after making the OSD on the current horizontal scanning line.

6. The on-screen display unit according to claim 2, wherein said buffer comprises a dual-port RAM.

7. The on-screen display unit according to claim 2, wherein said buffer transfer control circuit reads in advance at least two characters in each display duration of one character from among the data stored in said OSD RAM in a sequence to be displayed on the horizontal scanning line.